# Instruction Pipeline Execution Timeline

The following table illustrates the execution timeline for a sequence of instructions in a 5-stage pipelined RISC-V CPU. The stages are IF (Instruction Fetch), ID (Instruction Decode), EX (Execution), MEM (Memory Access), and WB (Write Back). Pipeline stalls, if any, are noted.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| add s0, s1, s2 | IF | ID | EX | MEM | WB |  |  |  |  |  |
| lw t0, 0(t1) |  | IF | ID | EX | MEM | WB |  |  |  |  |
| sw t2, 0(t3) |  |  | IF | ID | EX | MEM | WB |  |  |  |
| bne s0, s1, EXIT |  |  |  | IF | ID | EX | MEM | WB |  |  |

This timeline assumes no pipeline hazards or delays except for instruction dependencies implied by the sequence. Any branching or load-use hazards are managed by stalling or forwarding.